# N-Channel 100-V (D-S) MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
| 100 | 0.034 @ $V_{GS}$ = 10 V | 7.8 |
| | 0.040 @ $V_{GS}$ = 6.0 V | 7.2 |

## FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100 % $R_g$ Tested

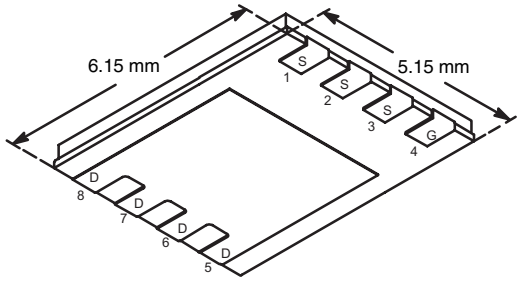
Pb-free Available

RoHS* COMPLIANT

## APPLICATIONS

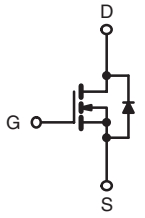
- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V, Full-/Half-Bridge DC/DC
- Industrial and 42-V Automotive

**PowerPAK® SO-8**




Bottom View

**Ordering Information:** Si7454DP-T1
Si7454DP-T1—E3 (Lead (Pb)-Free)




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | | | |
|---|---|---|---|---|---|
| Parameter | | Symbol | 10 secs | Steady State | Unit |
| Drain-Source Voltage | | $V_{DS}$ | 100 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | | |
| Continuous Drain Current ($T_J$ = 150°C)[a] | $T_A$ = 25°C | $I_D$ | 7.8 | 5.0 | A |
| | $T_A$ = 85°C | | 5.7 | 3.6 | |
| Pulsed Drain Current | | $I_{DM}$ | 30 | | |
| Avalanche Current | L = 0.1 mH | $I_{AS}$ | 25 | | |
| Single Avalanche Energy (Duty Cycle ≤ 1 %) | | $E_{AS}$ | 31 | | mJ |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | 4.0 | 1.6 | A |
| Maximum Power Dissipation[a] | $T_A$ = 25°C | $P_D$ | 4.8 | 1.9 | W |
| | $T_A$ = 85°C | | 2.6 | 1.0 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | –55 to 150 | | °C |
| Soldering Recommendations (Peak Temperature)[b,c] | | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient[a] | t ≤ 10 sec | $R_{thJA}$ | 21 | 26 | °C/W |
| | Steady State | | 55 | 65 | |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 1.6 | 2 | |

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile ( *http://www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

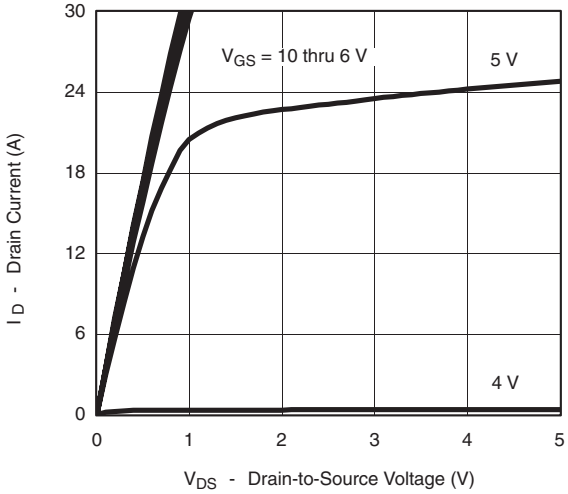
* Pb containing terminations are not RoHS compliant, exemptions may apply.

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Min** | **Typ** | **Max** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | | | 20 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 30 | | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 7.8 A | | 0.028 | 0.034 | Ω |
| | | $V_{GS}$ = 6.0 V, $I_D$ = 7.2 A | | 0.032 | 0.040 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 7.8 A | | 25 | | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 4 A, $V_{GS}$ = 0 V | | 0.8 | 1.2 | V |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_D$ = 7.8 A | | 24 | 30 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 7.6 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 5.4 | | |
| Gate Resistance | $R_g$ | | 0.5 | 1.25 | 2.2 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 50 Ω<br>$I_D \cong$ 1.0 A, $V_{GEN}$ = 10 V, $R_G$ = 6 Ω | | 16 | 30 | ns |
| Rise Time | $t_r$ | | | 10 | 20 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 35 | 70 | |
| Fall Time | $t_f$ | | | 20 | 40 | |
| Source-Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 4 A, di/dt = 100 A/µs | | 50 | 80 | |

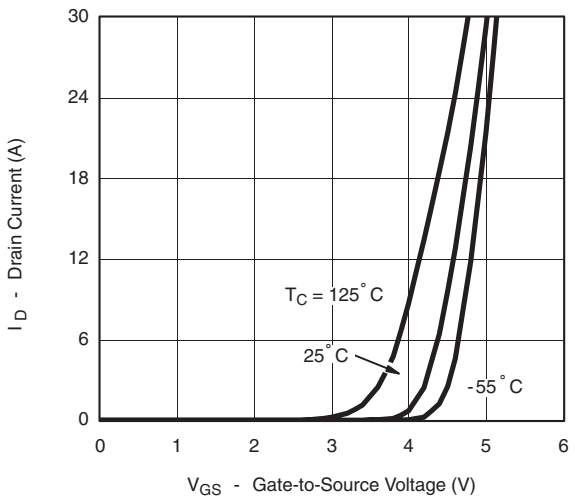
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## TYPICAL CHARACTERISTICS 25 °C, unless noted

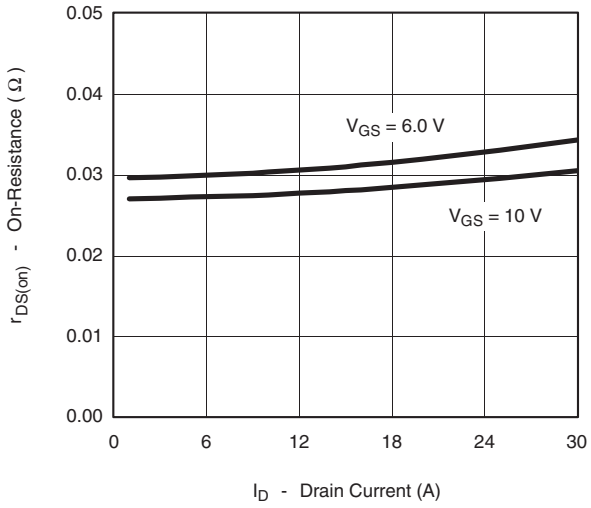



**Output Characteristics**

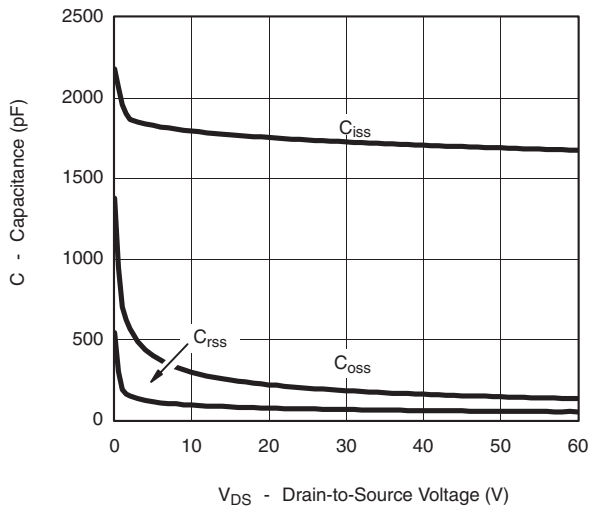



**Transfer Characteristics**

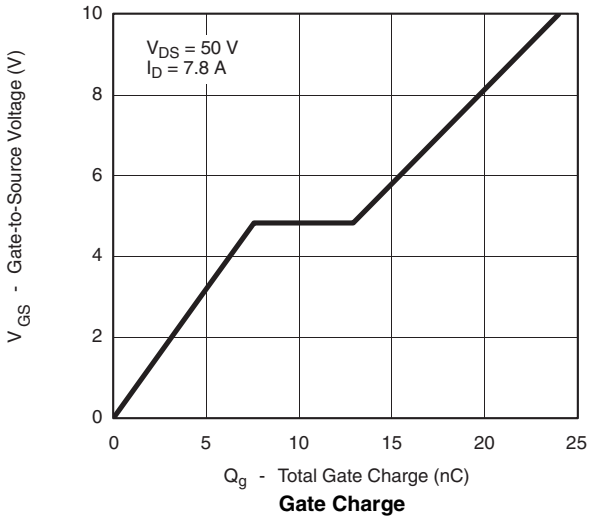
## TYPICAL CHARACTERISTICS 25 °C, unless noted



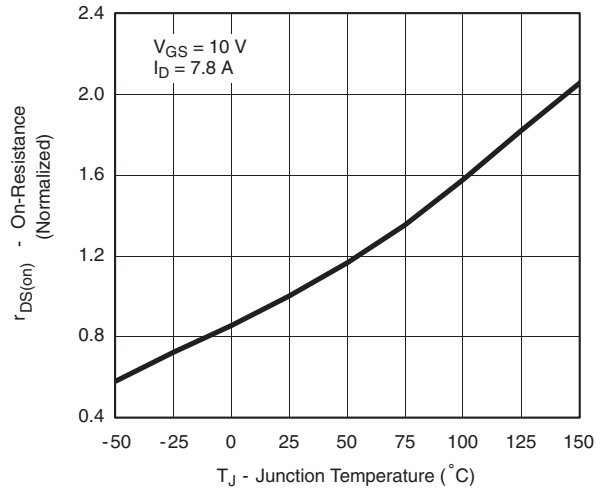

**On-Resistance vs. Drain Current**



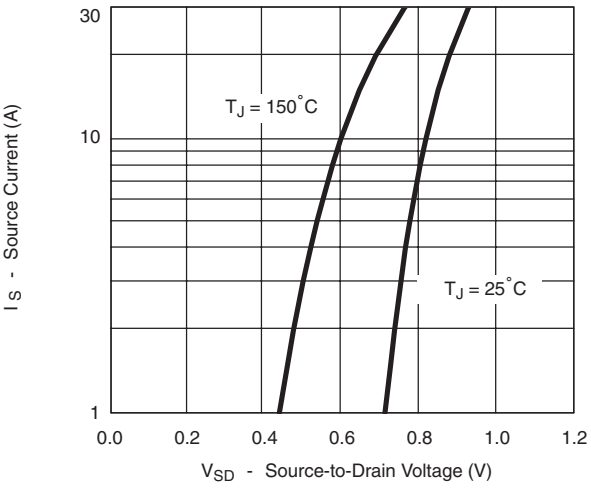

**Capacitance**



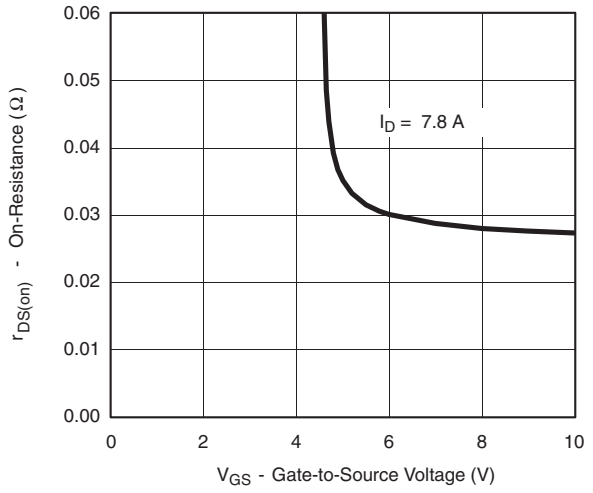

**Gate Charge**




**On-Resistance vs. Junction Temperature**

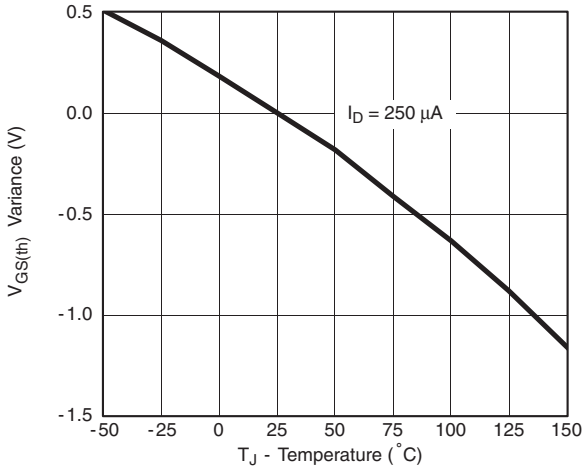



**Source-Drain Diode Forward Voltage**

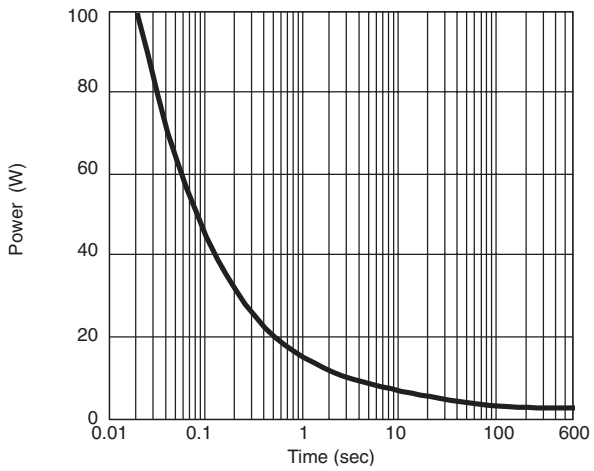



**On-Resistance vs. Gate-to-Source Voltage**

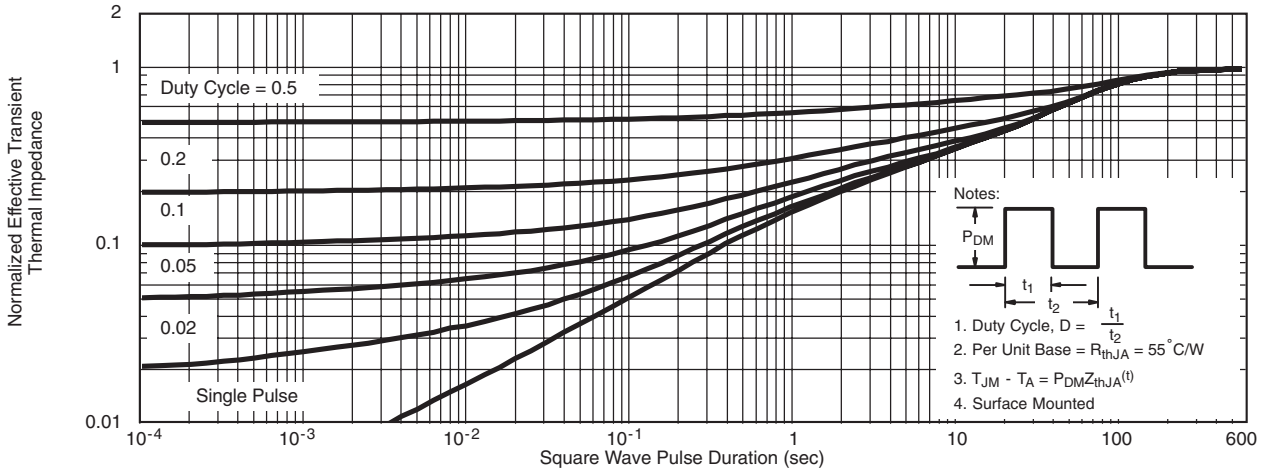
## TYPICAL CHARACTERISTICS 25 °C, unless noted



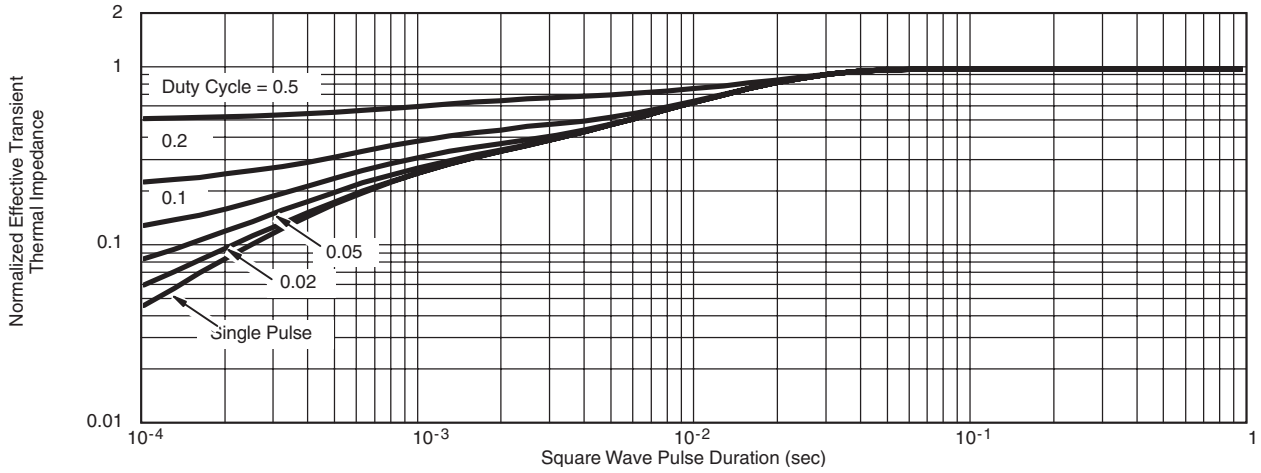

**Threshold Voltage**




**Single Pulse Power**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Case**

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